Name:	1.0us	2.0us	3.0us	4.0us	5.0us	6.0us	7.0us	8.0us	9.0us	10.0us	11.0us	12.0
[I] RFCIk												
[I] RevolutionClock												
[I] RotDelayDone												
[I] DelayedRevolutionClock												
[I] BucketCounterEnable												
[I] BunchFillMask												
[O]FineCounterEnable												
[O]FineCounterClock												
[B] TriggerCounterEnable												
[I] Output					M							
		Counter set to 0x										
	Revolution Counter set to 0x0010.											
	Trigger Counter Clock Selector set to GND (No Stop).											
	Fine Counter Clock Selector set to Fixed,											
	Bucket Counter Enable Selector set to Revolution Counter Terminal Count,											
	Revolution Counter Enable Selector set to Event.											
	This channel will output a continuous 9.37MHz Clock.											
	There is no Trigger Counter Terminal Count (Halt Trigger). Reconfiguring of channel can be accomplished by											
	a VMEbus Command.											
	FineDelayClock can be	nhased shifted in	increments of 50	Ons to vield the	output triggers							
	I mobolay clock dair bo	priacoa crimoa ii		sopo to yiola tilo	output inggoro.							
	Timing Diagram #3 - Co	ntinuous 9.37MH	z output no Halt									
	3 23 27											